WE CLAIM:

1. A method of connecting SONET/SDH termination devices with payload processing devices, comprising:

(a) providing a transmit interface operative to receive incoming SONET/SDH signal streams and convert said SONET/SDH signal streams into outgoing low voltage differential signal (LVDS) levels with said SONET/SDH signal streams mapped into 8B/10B control characters so as to label SONET/SDH frame boundaries; and

(b) providing a receive interface operative to receive incoming LVDS signal levels and convert said LVDS signal levels into outgoing SONET/SDH signal streams with decoding of said 8B/10B control characters labeling SONET/SDH frame boundaries into SONET/SDH control signals.

2. A method according to claim 1, wherein said SONET/SDH frame boundaries include transport frame, high-order path frame and low-order path frame boundaries.

3. A method according to claim 1, including mapping a descrambled SONET/SDH data stream into 8B/10B control

characters to ensure data transitions on serial links and to preserve DC balance.

4. A method according to claim 1, including treating positive and negative disparity codes of said 8B/10B control characters having an even number of ones and zeros as separate control characters.

5. A method according to claim 1, including storing signals in a buffer and transferring said signals using a universal frame pulse with a software programmable delay to allow transfer of one or more SONET/SDH signals over multiple links.

6. A method according to claim 1, including providing transparent in-band error reporting where errors detected at a SONET/SDH receiver can be transferred to a transmitter to construct remote error and defect indication codes.

7. A method according to claim 1, including inserting a pseudo-random bit sequence pattern in serial transmit links to allow data path verification prior to injection of actual payload.

8. A method according to claim 1, including using line code violations of 8B/10B characters to monitor error performance of serial links.

9. A method according to claim 1, including overwriting one of the E1 and B1 bytes to form a pattern which allows in-service monitoring of link functionality as well as monitoring of downstream cross-connect mis-configurations.

10. A method according to claim 9, wherein bytes in E1 are overwritten with a complement of a value in B1 bytes.

11. A bus interface device for connecting SONET/SDH termination devices with payload processing devices, comprising:

(a) a transmit interface operative to receive incoming SONET/SDH signal streams and convert said SONET/SDH signal streams into outgoing low voltage differential signal (LVDS) levels with said SONET/SDH signal streams mapped into 8B/10B control characters so as to label SONET/SDH frame boundaries; and

(b) a receive interface operative to receive incoming LVDS signal levels and convert said LVDS signal

levels into outgoing SONET/SDH signal streams with decoding of said 8B/10B control characters labeling SONET/SDH frame boundaries into SONET/SDH control signals.

12. A bus interface device according to claim 11, wherein said SONET/SDH frame boundaries include transport frame, high-order path frame and low-order path frame boundaries.

13. A bus interface device according to claim 11, including a plurality of 8B/10B encoder blocks operative to map a descrambled SONET/SDH data stream into 8B/10B control characters to ensure data transitions on serial links and to preserve DC balance.

14. A bus interface device according to claim 11, including a buffer for storing signals, wherein said signals are transferred using a universal frame pulse with a software programmable delay in order to allow transfer of one or more SONET/SDH signals over multiple links.

15. A bus interface device according to claim 11, including a pseudo-random bit sequence generator operative to insert a pseudo-random bit sequence pattern into serial transmit links to allow data path verification prior to injection of actual payload.

16. A bus interface device according to claim 11, including a character alignment block and a frame alignment block operative to detect line code violations of 8B/10B characters in order to monitor error performance of serial links.

17. A bus interface device according to claim 11, including a pseudo-random bit sequence detector operative to monitor and overwrite E1 and B1 bytes to form a pattern which allows in-service monitoring of link functionality as well as monitoring of downstream cross-connect mis-configurations.

18. A bus interface device according to claim 17, wherein bytes in E1 are overwritten with a complement of a value in B1 bytes.